MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

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MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

Summary

This contract seeks to develop a family of thin-film stimulating arrays for use in neural prostheses. STIM-2B/-3B are two- and three-dimensional arrays of stimulating sites on 400μm centers. The probes have four channels and 64-sites. Any selected site can be used for either recording or stimulation. Current generation is off-chip. This probe design has now been completed, with 3D arrays of the STIM-3B probes formed in arrays as large as 1024 sites (256 shanks and 64 parallel data channels, accessible over just eleven external leads). The high-end probes STIM-2/-3 are similar except they use on-chip current generation via 8-bit digital to analog converters. They are accessible over seven external leads.

During the past quarter, work under this program completed the fabrication of STIM-2 and STIM-3 probes as well as the platform address-decoding chip mentioned in the previous quarterly report. As of this writing, the probes are being tested at wafer level, and indications are that the fabrication run was completely successful. Thresholds are on target and all circuitry appears functional. We will perform detailed wafer-level testing prior to moving to final etch-out of the probes and then in-vitro and in-vivo testing.

A wireless interface for the STIM-2/-3 stimulating probes has also been fabricated and is being tested. In addition, many of the elements of this interface have been integrated on a chip aimed at use with simple passive stimulating probes. The chip contains an interface for four stimulating sites, each of which can be put in a number of states. In addition to circuit blocks taken from the STIM-2/-3 interface, new circuit blocks aimed at interfacing with passive probes have been used, including site drivers, digital-to-analog converters, and digital control circuits. The intent here is to be able to demonstrate and soak-test (in-vivo) a simple interface using this system and then moved to full wireless tests using STIM-2 and STIM-3. We hope to report the first of these tests in the next report.

MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

1. Introduction

The goal of this contract is the development of active multi-channel arrays of stimulating electrodes suitable for studies of neural information processing at the cellular level and for a variety of closed-loop neural prostheses. The probes should be able to enter neural tissue with minimal disturbance to the neural networks there and deliver highly-controlled (spatially and temporally) charge waveforms to the tissue on a chronic basis. The probes consist of several thin-film conductors supported on a micromachined silicon substrate and insulated from it and from the surrounding electrolyte by silicon dioxide and silicon nitride dielectric films. The stimulating sites are activated iridium, defined photolithographically using a lift-off process. Passive probes having a variety of site sizes and shank configurations have been fabricated successfully in past contracts and have been distributed to a number of research organizations nationally for evaluation in many different research preparations. For chronic use, the biggest problem associated with these passive stimulating probes concerns their leads, which must interface the probe to the outside world. Even using silicon-substrate ribbon cables, the number of allowable interconnects is necessarily limited, and yet a great many stimulating sites are ultimately desirable in order to achieve high spatial localization of the stimulus currents.

The integration of signal processing electronics on the rear of the probe substrate (creating an "active" probe) allows the use of serial digital input data that can be de-multiplexed on the probe to provide access to a large number of stimulating sites from a very few leads. Our goal in this area is to develop a family of active probes capable of chronic implantation in tissue. For such probes, the digital input data must be translated on the probe into per-channel current amplitudes that are then applied to tissue through the sites. Such probes generally require five external leads, virtually independent of the number of sites used. As discussed in previous reports, we have designed a series of active probes containing CMOS signal processing electronics. Two of these probes have been completed and are designated as STIM-1A and STIM-1B. A third probe, STIM-2, is now beginning a final iteration and is a second-generation version of our original high-end first-generation design, STIM-1. All three probes provide 8-bit resolution in digitally setting the per-channel current amplitudes. STIM-1A and -1B offer a biphasic range using $\pm 5V$ supplies from 0µA to ± 254µA with a resolution of 2µA, while STIM-2 has a range from 0 to ± 127µA with a resolution of 1µA. STIM-2 offers the ability to select 8 of 64 electrode sites and to drive these sites independently and in parallel, while STIM-1A allows only 2 of 16 sites to be active at a time (bipolar operation). STIM-IB is a monopolar probe, which allows the user to guide an externally-provided current to any one of 16 sites as selected by the digital input address. The high-end STIM-2 contains provisions for numerous safety checks and for features such as remote impedance testing in addition to its normal operating modes. It also offers the option of being able to record from any one of the selected sites in addition to stimulation. It will be the backbone of a

multi-probe three-dimensional (3D) 1024-site array (STIM-3) now in development. A new probe, STIM-2B, has recently been added to this set. It offers 64-site capability with off-chip generation of the stimulus currents for four separate channels. These channels are organized in four groups so that each current can be directed to any of the 16 sites in its group. Each selected channel can be programmed for either stimulation or recording. On-chip recording amplifiers offer a gain of 50; alternatively, the neural activity can be recorded using off-chip amplifiers interfaced through the normal stimulating channels. This probe is available in both 2D and 3D versions (as STIM-2B/3B) and is now being used in-vivo.

During the past quarter, we have focused work on the fabrication of the STIM-2 and STIM-3 probes as well as a new wireless interface for them. The results of these efforts are described more fully in the sections below.

2. STIM-2/3: A Multiplexed Stimulating Probe with On-Chip Current Generation

As noted during the previous quarterly report, we have completed the design of modified STIM-2 and STIM-3 probes. The specifications of STIM-2 are given below in Table 1 along with the performance specifications for its on-chip recording amplifier. The modified probe has seven external leads (VDD, GND, VSS, CLK, STB, Data In, and (analog) Data Out. It features a new digital-to-analog converter (DAC) with improved performance as well as extensive self-test capabilities to allow the probe to be tested automatically prior to microassembly in 3D arrays (STIM-3).   The probe is configured with eight shanks having 8 sites per shank, with the sites spaced at 200µm intervals in depth and the shanks spaced laterally at 400µm. One of the concerns associated with this probe is the relatively large layout area devoted to the circuitry. This makes the back of the probe appreciably wider than the span allotted to the shanks and the vertical rise above the cortex more than twice the 1mm height desired for a chronic implant. Figure 1 shows the layout of STIM-3. If the probe were fabricated in a more aggressive technology having a 1µm feature size, or a 0.5µm feature size, as compared to our present 3µm university process, the circuit dimensions would be reduced by linear factors of three to six and would be consistent with in-vivo use. However, in the meantime we continue to consider options for reducing the circuit size.

One means of minimizing the vertical height of the implant is to fold the circuit area over flat against the cortex. This has been explored previously in mock-up versions and has been implemented in some of the versions of STIM-3 now being fabricated as shown in Fig. 1. This design uses silicon ribbon cables to form flexible bridges between the rigid shanks and 3D mounting wings and the back circuit area. This design will allow us to see if this fold-down structure really works. The use of silicon ribbon cables for the flexible bridges provides structures that can be well insulated but which can not be bent through radii of less than about 300µm without risk of breakage. Gold-plated beams are also a possibility. They are not "springy" and can be bent through radii of less than 30µm but would have to rely on the epoxy/silastic that is used to pot the assembly for

insulation. This is perhaps not a bad choice for a stimulating probe and will be explored in the future depending on the performance of the silicon cables.

Table 1: Specifications for STIM-2/-3

Process technology	Bulk micromachined 3um n-epi, p-substrate, p-well CMOS process
Power supplies	Vcc=5V, Vss=-5V, GND=0V
Current range	±127 µA with 1uA resolution
Total circuit area	5.8mm * 2.5mm
Total external leads	7 (Vcc, Vss, GND, Clock, Data_in, Data_out, STB)
Shank dimension	104µm (Width) , 3.3mm(Length)
Shank spacing	400µm
No. of shank	8
No. of sites per shank	8
Site area	1000µm^2
Site spacing	200µm

Gain	40dB
Bandwidth	3.2Hz~14kHz
Power consumption	212.1µW
Input reference noise	7.93µVrms

During the past quarter, the primary focus of activity was to fabricate the acute and chronic STIM-2/3 probes along with a platform-based interface chip for use with the STIM-3 arrays. This platform chip is shown in Fig. 2 in layout form and masks the strobe (STB) signal from all but the addressed probe in a 3D array. As of this writing, the new probes and the platform chip are undergoing wafer-level testing, prior to final etch-out and use in-vivo. The thresholds appear to be on target and we are optimistic that we will have working probes for in-vivo use. Figures 3 and 4 show the STIM-3 probe on the wafer.
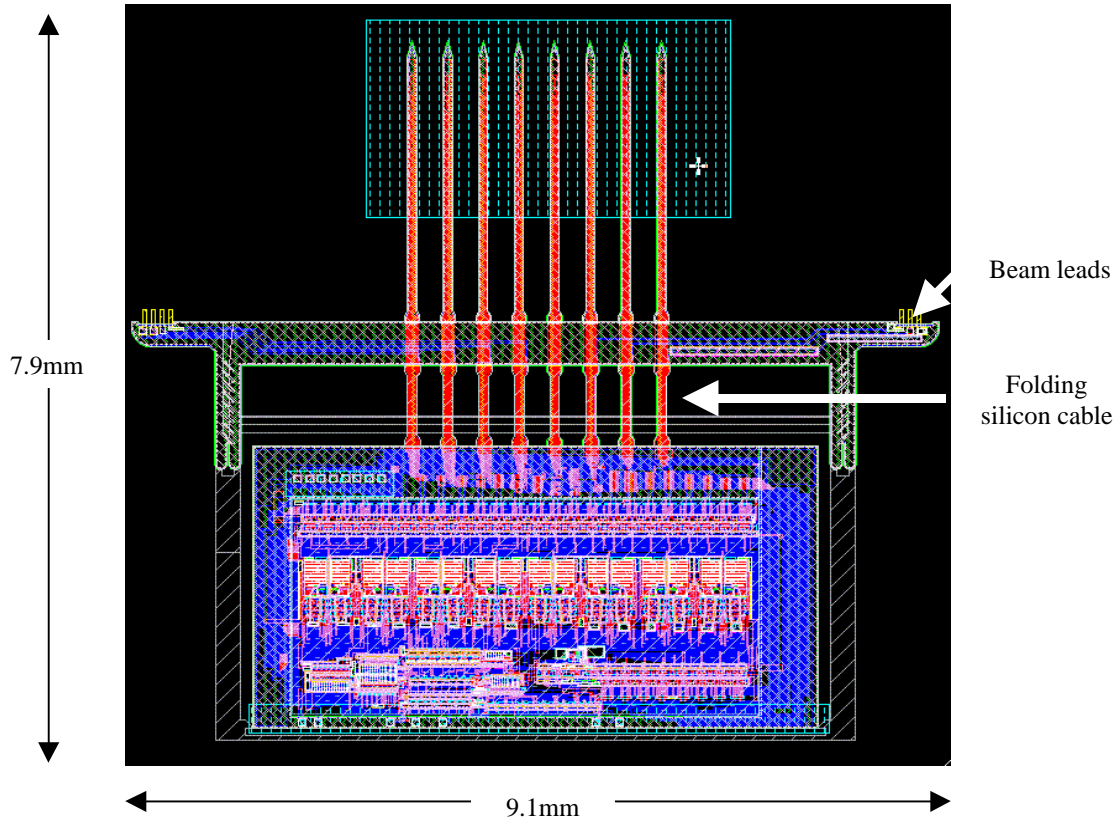
Fig. 1: Layout of STIM-3. The shaded blocks around the probe indicate where dielectric compensation is being used.
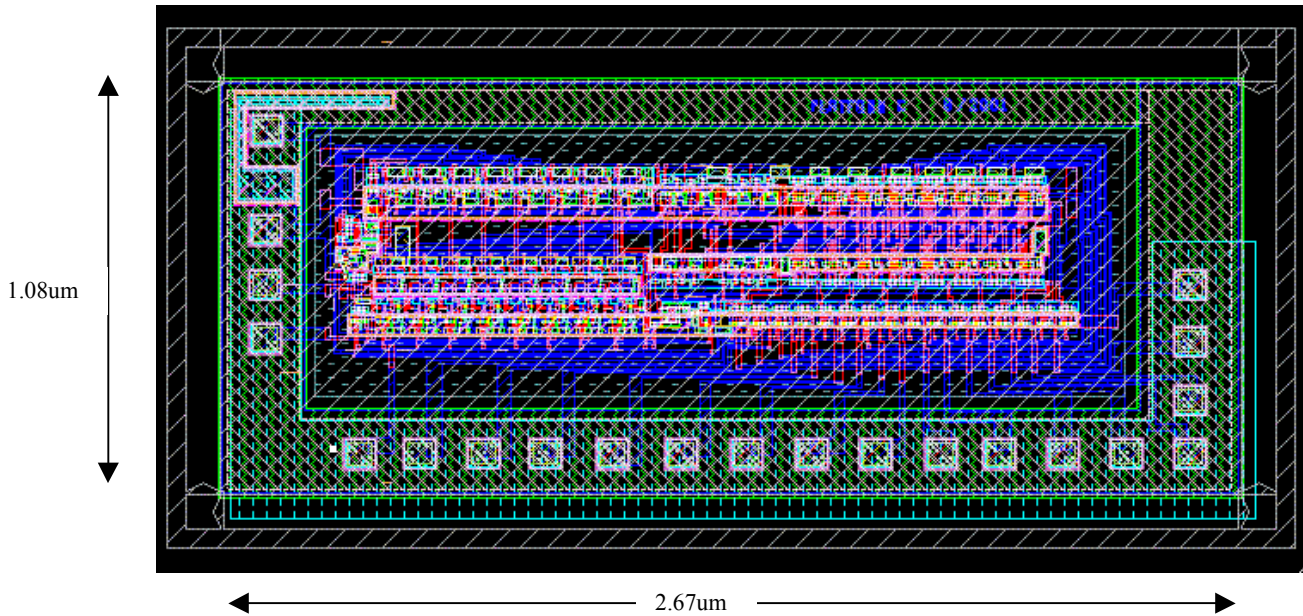

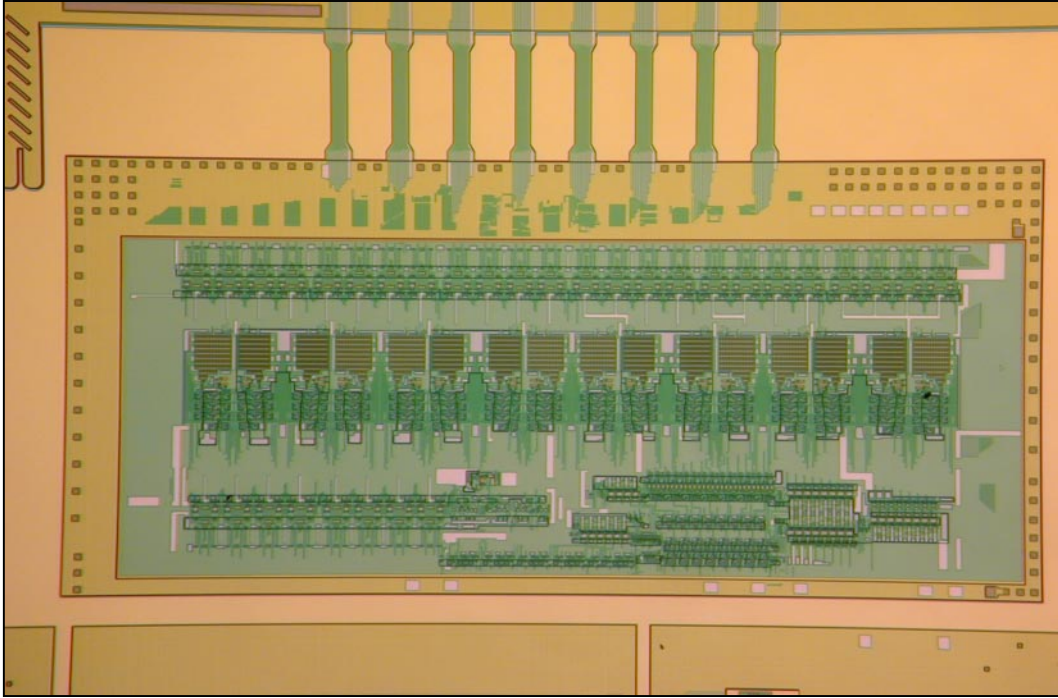Fig. 2: Layout of the platform addressing chip to be used with STIM-3

Fig. 3: Photograph of the back-end circuitry on the new STIM-3 probe. The probe is shown after poly definition but before final metal.
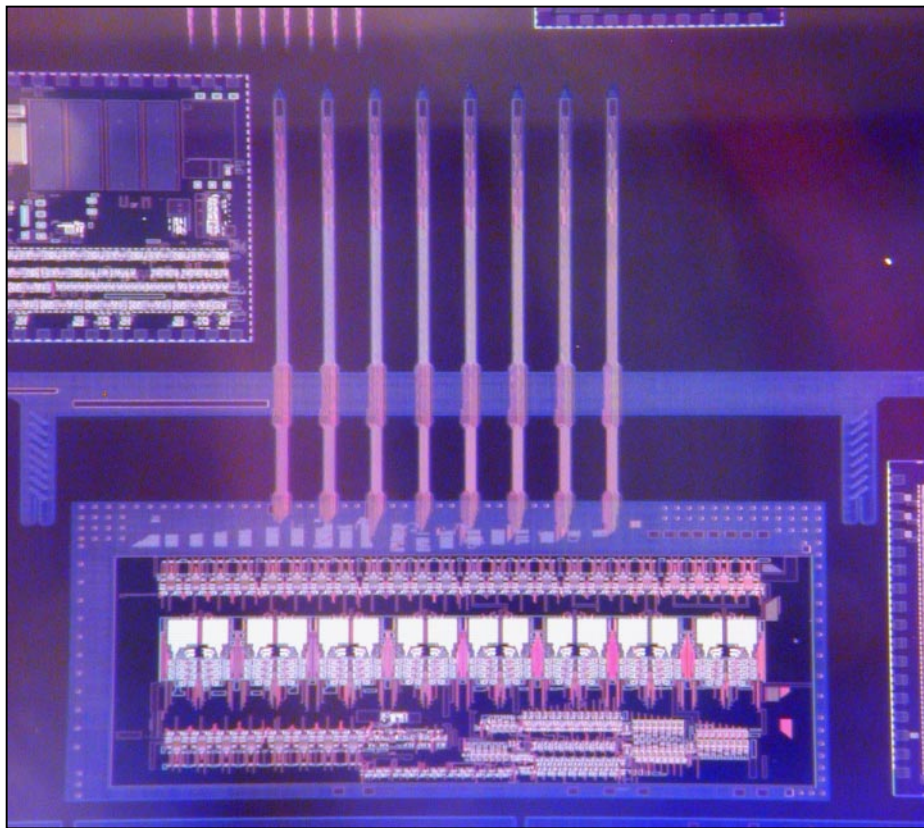

Fig. 4: Photograph of the overall STIM-3 probe, taken just prior to wafer-level testing.

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Another possible approach that would help minimize the circuit area would be to remote some of this circuitry to the platform chip, which could be fabricated in a commercial foundry using a standard CMOS process and tighter design rules. Partitioning the circuitry with the input registers on the platform chip would make sense but would absorb relatively little of the circuit area. The selection matrix would absorb more, but the increase in interconnect count (from 7 to 71) would be prohibitive. The DACs probably represent the most viable target. Placing them on the interconnect chip would add eight additional leads per probe between the probe and the platform (from 7 to 15) but would probably be manageable; however, it might complicate the self-test connections considerably . The savings in circuit area would be substantial, however, and would likely avoid having to fold the circuit areas of the probe over, so this is being examined to understand its suitability for a subsequent version of this probe. Full test results on the present probe design will be presented in the next quarterly report.

3.   A Wireless CNS Stimulating System

A Complete Telemetry Interface Chip

Design of the first complete telemetry interface chip, INTERESTIM1, was completed during the previous quarter (Apr-Jun 2001) by putting individual blocks together as shown in Fig. 5 and by completing the interface chip layout as well as doing final simulations, including parasitic effects. This chip has been designed to be implanted and provide a wireless link between STIM-2/-3 and an external system that processes visual or auditory information and transmits it by modulating the electromagnetic power carrier signal. These are three major building blocks of a wireless CNS stimulating system.

To achieve a near-term fully wireless stimulating system, we have also designed a simpler stand-alone stimulator chip with four stimulation sites that can be used with passive stimulating probes. This system is specifically designed for a wireless implant and benefits from most of INTERESTIM1 RF front-end blocks, minimizing development time. This new stimulator is named INTERESTIM2, and its block diagram is shown in Fig. 6.   All blocks on the left half of the diagram exist in INTERESTIM1 as well and have been previously described in our NIH quarterly reports. The rest of blocks are newly added to the chip and are reported in the following pages.

Site Driver Block

Each INTERESTIM2 site can be put in four states under control of two bits of the Site Control Register (SCR), which are fed into site driver block as shown in Fig. 6. These four states do all of stimulation functions with a large degree of freedom. These are shown in Fig. 7 and are summarized in Table 3. A Power-On Reset (POR) circuit resets all of the registers at startup, so all of the sites are at high-Z state (0), which is a safe mode to start with. For cathodic and anodic phases of each stimulation, any number of sites can be connected to VCC (state1) or current sink (state2) by loading the

appropriate command byte in SCR, while the rest of sites remain in the high-Z state. The stimulation current passes from VCC to current sink and switches back by the next command as described above. State 3 is designated for several purposes. The first purpose is to provide a simple way of charge balancing whenever it is needed (for example, after a certain number of biphasic stimulations) by shorting any number of sites together. This method is effective and used in cochlear implants. Second usage is to record neural activity or DC baseline from any single or combination of sites. INTERESTIM2 does not have a transmitter block in the current version but it will be added in later versions to provide feedback on tissue activity, site impedances and power supplies. The third purpose of the analog state is to apply back-bias potential, which is usually less than 1V, to any combination of sites to increase the charge injection capability of those sites. This block has not been added to the current version but it is shown in the Fig. 6 block diagram with dashed lines and will be added in later versions.
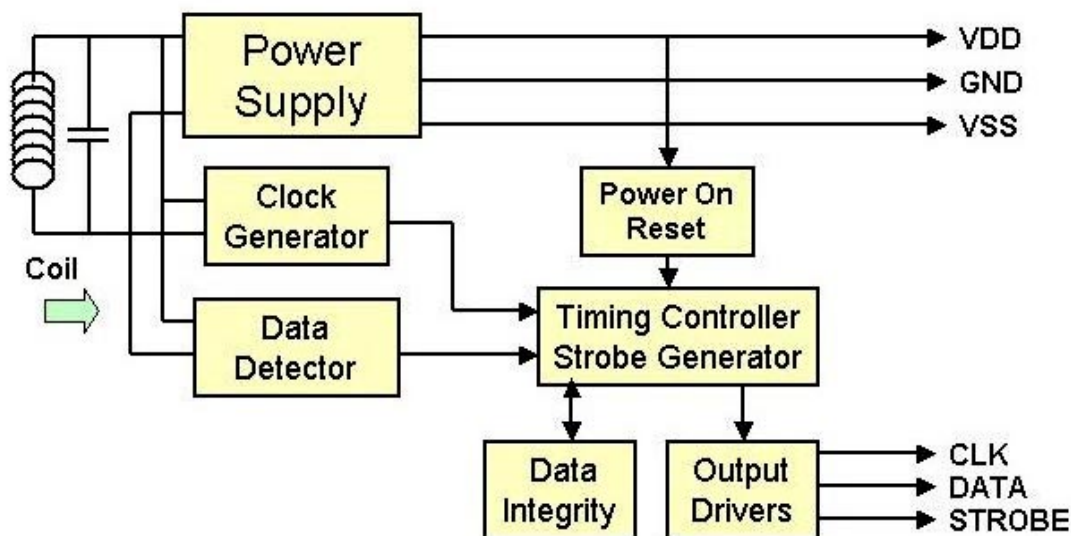

Fig. 5: Blocks present on the first version of the telemetry interface chip, INTERESTIM1.

The site driver circuit is shown in shown in Fig. 8. Transistors M1 and M2, which V_{gs} are controlled by an analog input voltage from the D/A converter block, provide a voltage-controlled current source (VCCS) for each site. The advantage of VCCS over the conventional scaled current-controlled current mirrors (CCCS) is its simplicity and small size particularly if we want to repeat it for each site. The disadvantage, on the other hand, is its non-linearity based on equation (1), which can be corrected by the external signal processor or by inverse non-linear weighting of D/A converter. This non-linearity might even be useful in some cases where smaller stimulation currents need to be tuned finer than large currents. Another disadvantage of VCCS is its vulnerability to process variations, which can change V_T and consequently affect I_d in (1). But CCCS based on transistor size ratios are more robust to process variations. We have tried to compensate for process variations by providing cutting links in the layout to fine-tune V_{gs} range after fabrication.
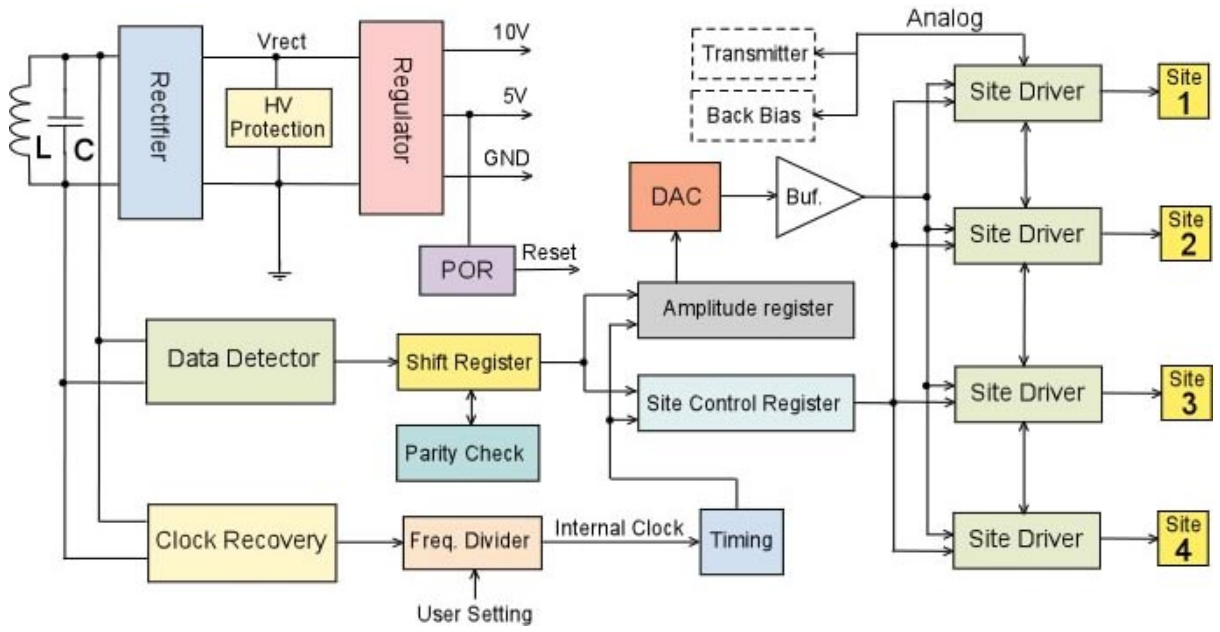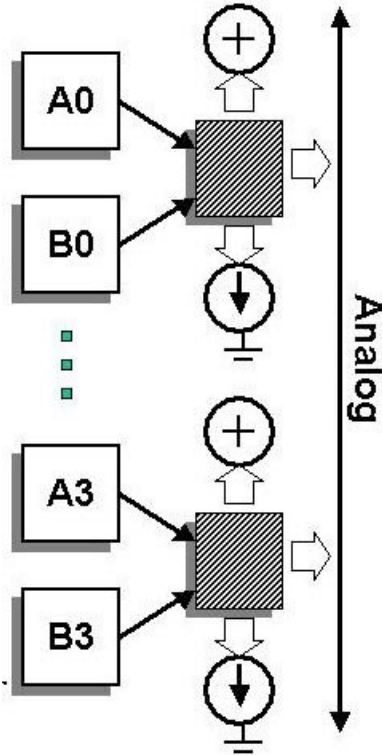
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Fig. 6: INTERESTIM2 block diagram.

Fig. 7: Stimulation mechanism in INTERESTIM2

Table 2: INTERESTIM2 site status and functions

State	A	B	Function	Description
0	0	0	High-Z	No connection
1	0	1	VCC	Connect to VCC
2	1	0	Sink	Connect to current sink
3	1	1	Analog	Connect to analog line
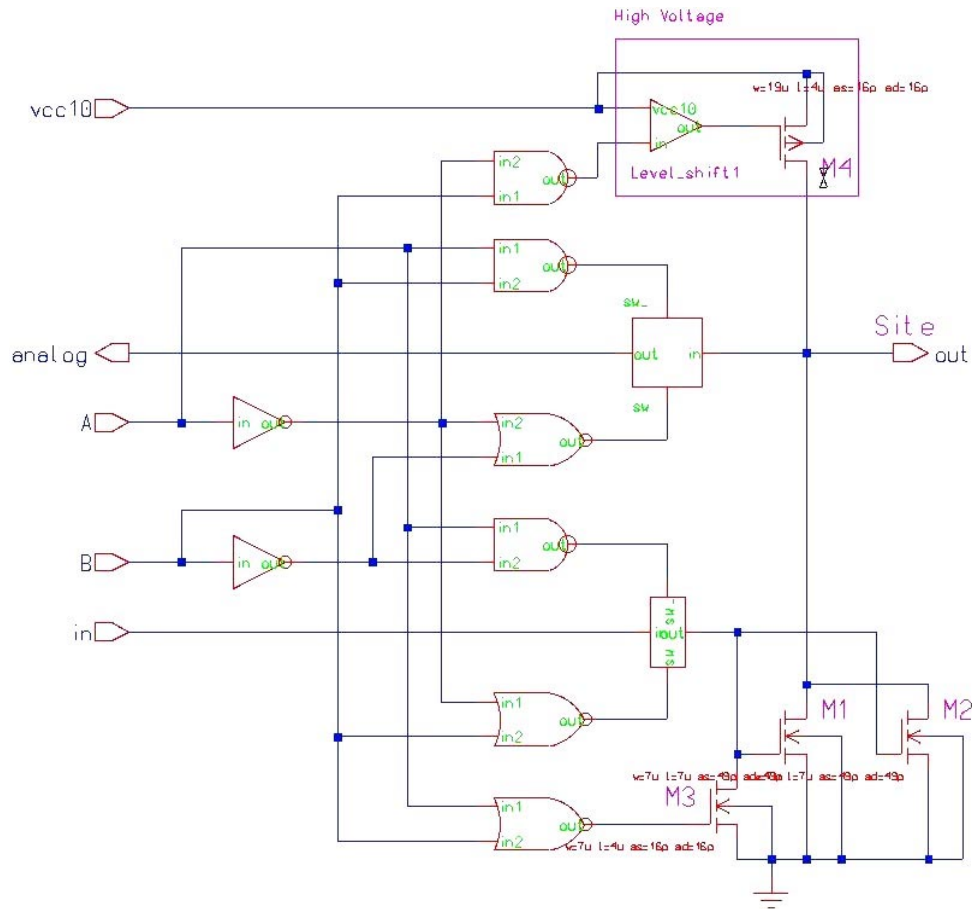
Fig. 8: Site Driver circuit schematic diagram
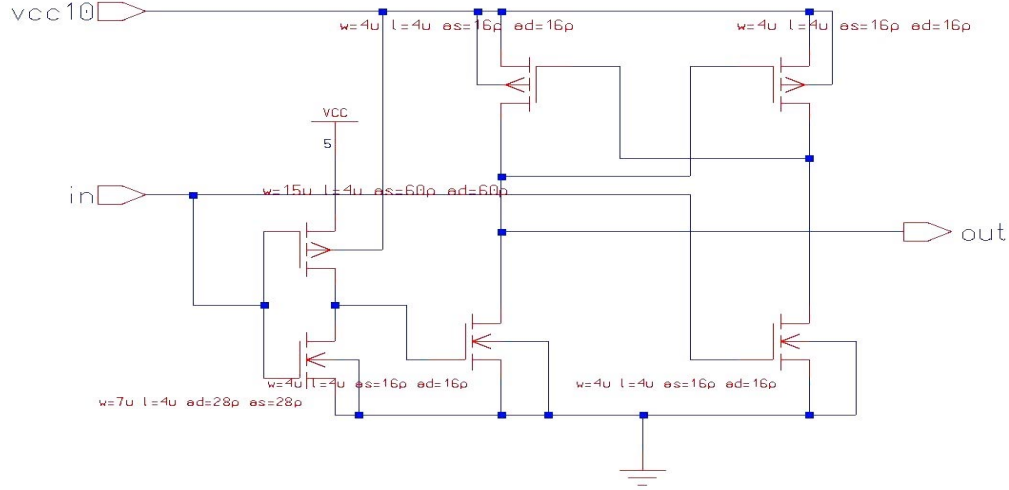
$$I_d = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_T)^2 \qquad (1)$$

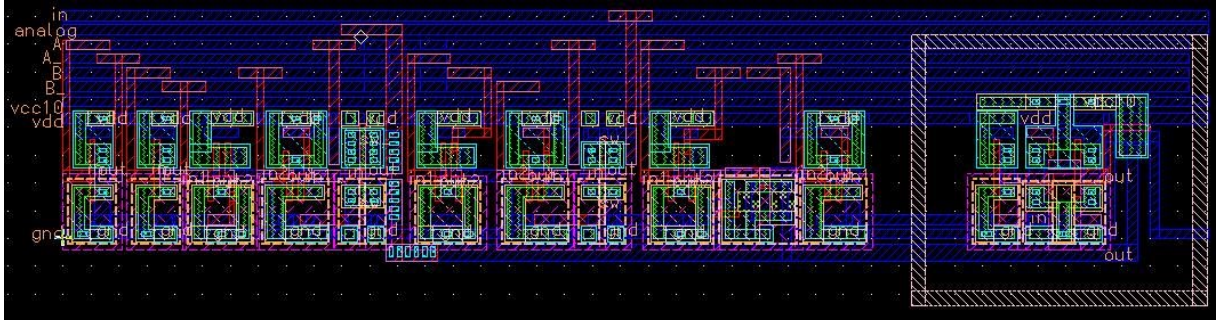Fig. 9: Digital level shifter circuit

Fig. 10: Site driver block layout

In state1, M1 and M2 gates connect to the analog input by a pass gate, and to adjust the stimulation current range, M1 or M2 can be open-circuited by cutting links. Transistor M4, which has a large W/L ratio, connects the site to VCC in state2. A level shifter circuit, which is shown in Fig. 9, controls M4 gate voltage digitally. This circuit is needed to change digital signals from 0-5V to 0-10V. The cross-coupled pair does not have any static power consumption and its transistors are chosen minimum size to minimize dynamic power. In state 0, M4 gate voltage is 10V to turn it off and M1 and M2 gates are grounded by M3, putting the stimulation site in high-Z status. Finally, each site is connected to common analog line by a large W/L pass gate in state 3 meanwhile other transistors are turned off. Fig. 10 shows site driver block layout.

Digital to Analog Converter:

The usual method for D-to-A conversion in microstimulators as mentioned in previous section is using scaled current mirrors as CCCS, which directly scale a reference current to provide stimulation current. The advantage of this method is its linearity and robustness against process parameter variation. But here, an analog voltage is needed to

control VCCS. Figure 11 shows a 7-bit DAC circuit, which uses serial as well as parallel minimum-sized PMOS transistors to scale the reference current. The advantage of this method over using only parallel transistors is a significant cut in circuit area in expense of some non-linearity because of the body effect in series PMOS transistors. The area, which is occupied by a 7 bit conventional DAC is $2430\mu m^2$ compared to only $460\mu m^2$ occupied by this circuit. Cutting links are added to the reference current branch to adjust the current range and compensate for any process variation.
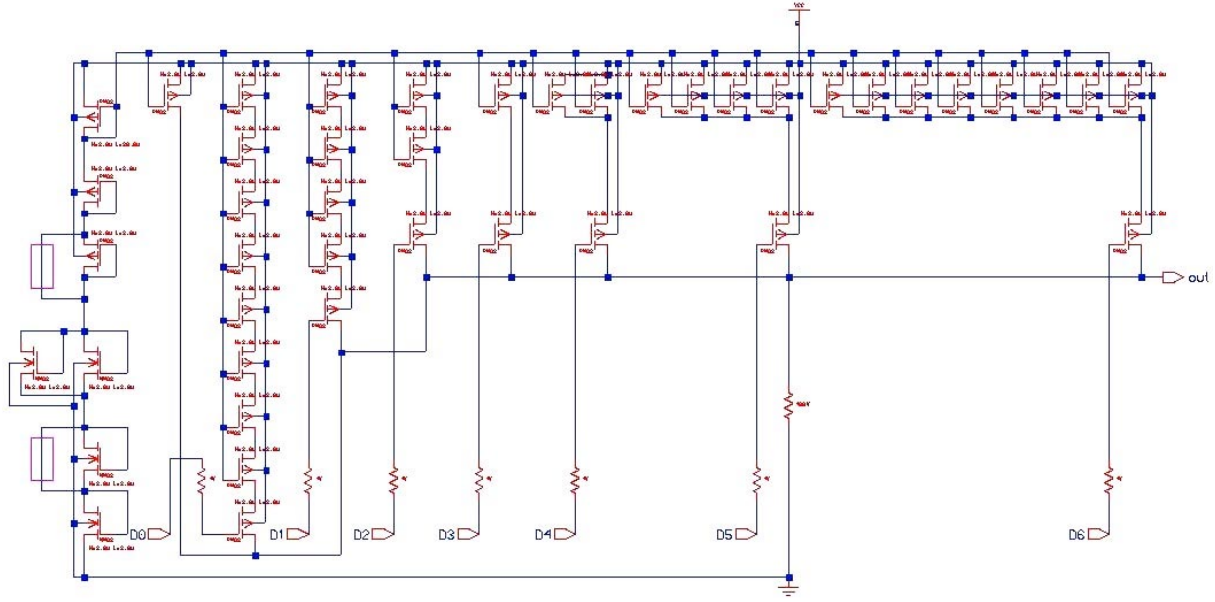

Fig. 11: 7-Bit digital to analog converter circuit

The DAC output cannot drive resistive or capacitive loads directly, so a unity gain buffer is added as shown in Fig. 6 to drive site driver capacitive loads. Classic 2-stage opamps with unity gain feedback as a buffer can source large currents into a load capacitor and charge it in a short transient time. But for discharging the load capacitor they are limited to second stage biasing current, which should be kept low for saving power. Hence, the falling transition would be too long for square stimulation pulse shapes. To solve this problem, a switch is added in parallel with the load capacitor to rapidly discharge it whenever the input is lower than the output more than a certain offset value as shown in Fig. 12. A small offset is needed to prevent this circuit from oscillation when the unity gain buffer keeps V_{out} equal to V_{in}.

The actual step follower circuit can be seen in Fig. 13. Transistors M9-M18 make a classic two-stage opamp, which is connected as a unity gain buffer. R1 and C1 are added for compensation and have significant effect on step response transient. M1-M5 are connected as a comparator, which output is square shaped by M6 and M7 inverter to drive M8 discharging switch. 50mV of offset is provided by R2 when I_{d18} bias current

passes trough it. This circuit consumes 57.5µW with 5V supply and is able to drive capacitive loads as high as 100pF with slew rate higher than 10^6 V/sec.
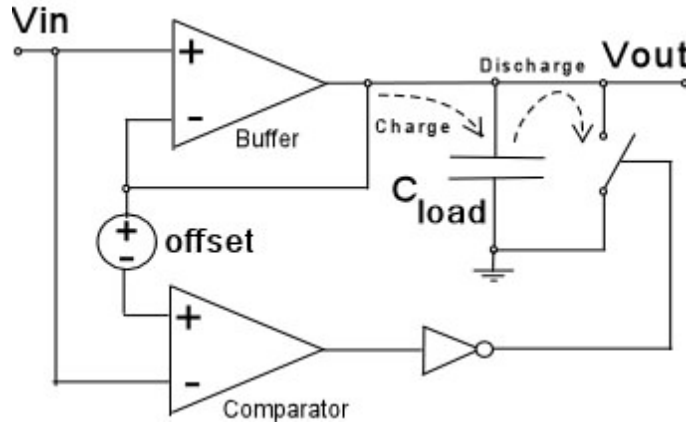
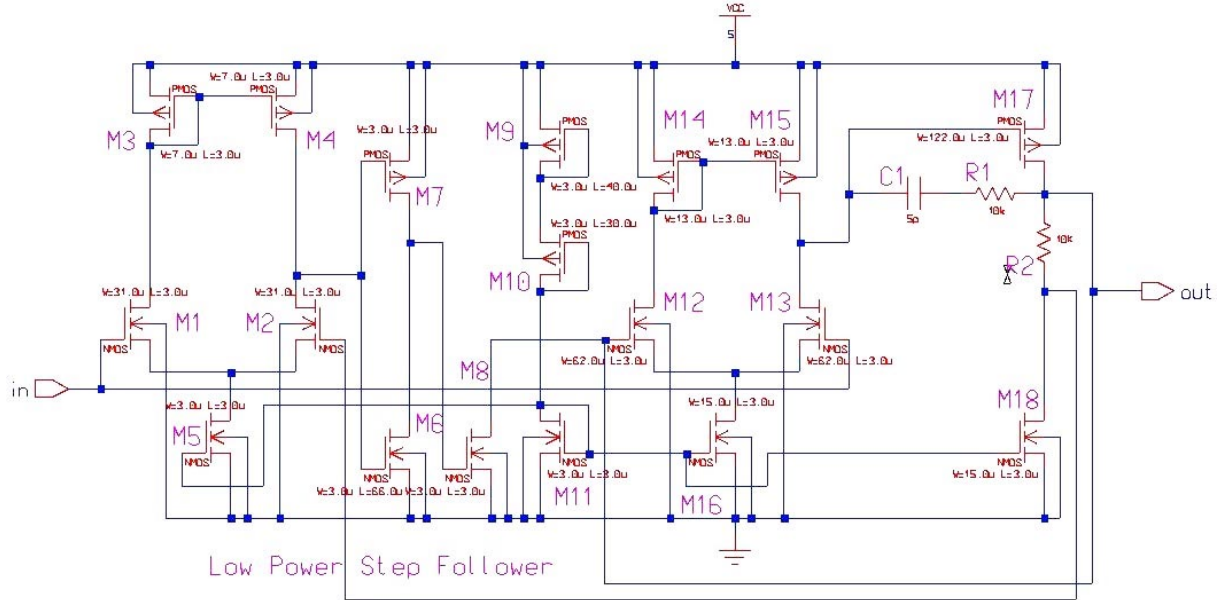

Fig. 12: Unity gain step follower schematic diagram

Fig. 13: Unity gain step follower circuit

Digital Block:

In the digital part of INTERESTIM2, the 9-bit shift register, parity check, user adjustable frequency divider and 5-bit timer are the same as INTERSTIM1. The timer block in INTERESTIM1 was used to generate strobe signals at 9th and 18th bits of each frame. INTERESTIM2 uses the same timing protocol with 18 bits in each frame. Each frame contains two command bytes and two parity bits as shown in Fig. 14. The first byte is for site status control and specifies the state of each of four sites with 2 bits per site based on Table 2. The second byte specifies the stimulation current amplitude with 7-bit resolution. Figure 15 shows INTERESTIM2 digital block circuit schematic. The 5-

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bit timer generates two signals, n8_ and n17_ at 9th and 18th clock cycles, respectively. These pulses are used to latch the shift register contents, which are site control and amplitude commands in to Site Control (SCR) and Amplitude (AMP) registers. So there is no change in these register values until the command bytes are loaded into the shift register and parity checked. As soon as command bytes are separated and loaded it to SCR and AMP, they become effective and change stimulator functionality. Figure 16 shows sample simulation waveforms of INTERESTIM2 digital block. Starting from the bottom trace, it shows internal clock, serial data bit stream and POR as well as n8_ and n17_ timing signals. The upper four traces show contents of the two least significant bits of SAR and AMP registers.
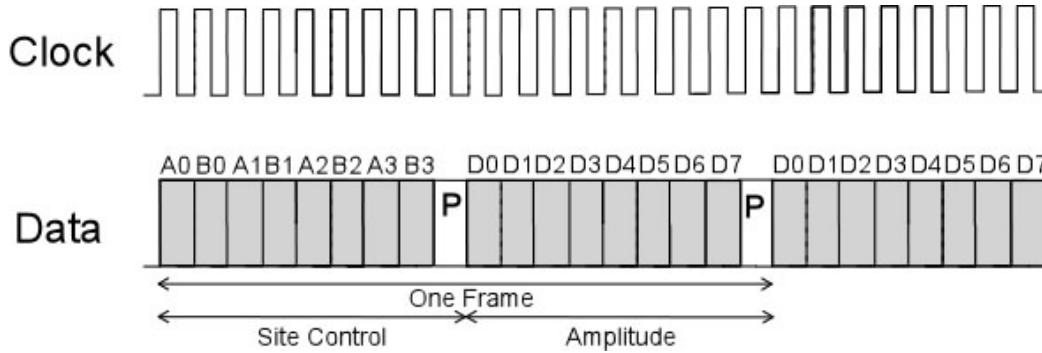

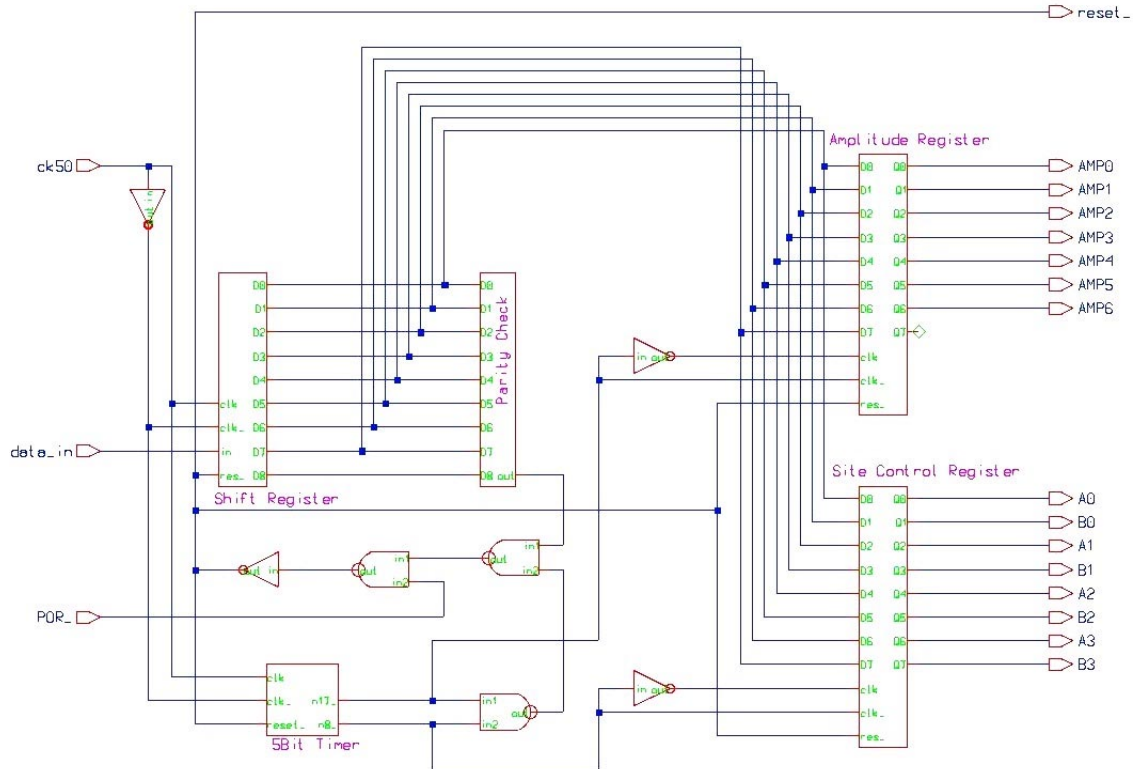Fig. 14: INTERESTIM2 timing protocol

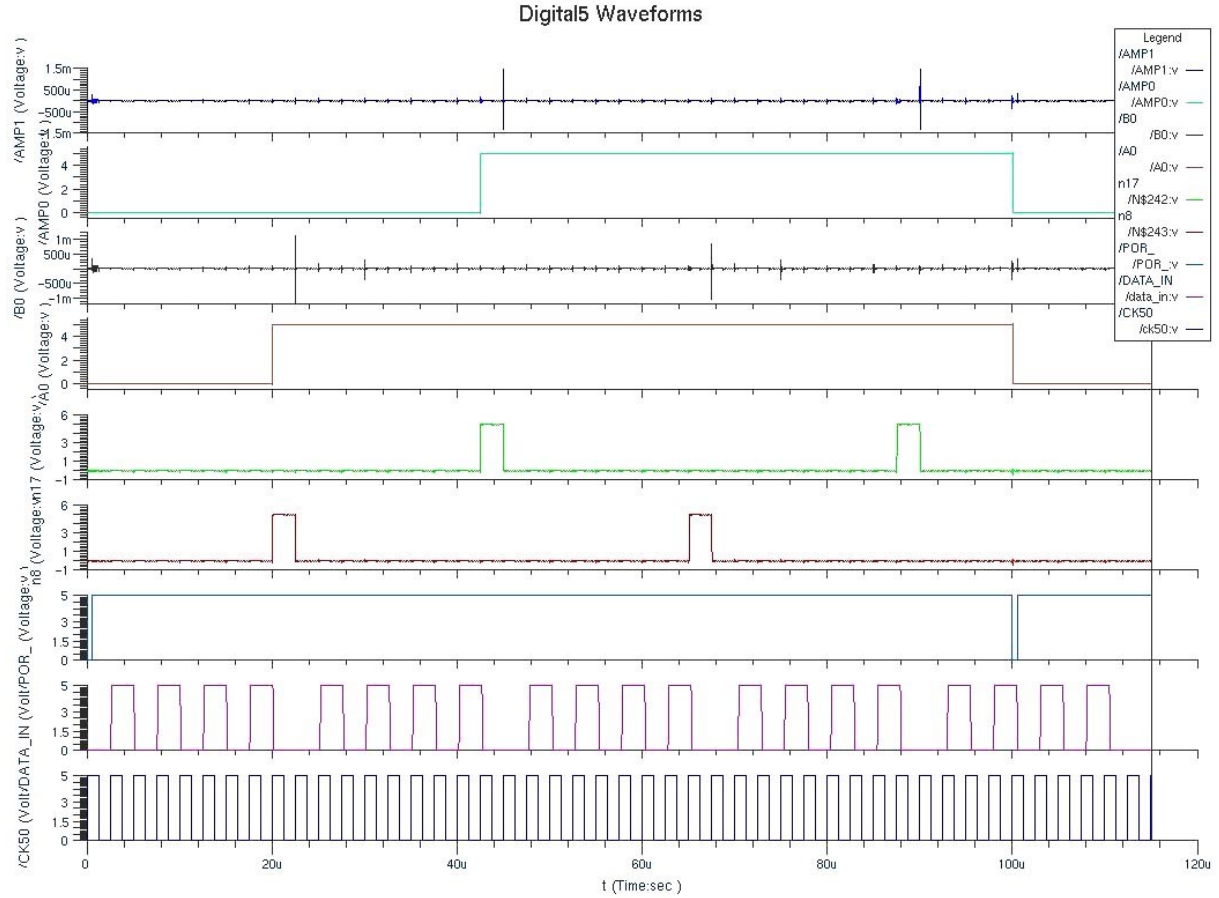Fig. 15: INTERESTIM2 digital block schematic circuit

Fig. 16: INTERESTIM2 digital block simulation waveforms

The complete circuit schematic of INTERESTIM2 can be seen in Fig. 17, which resembles the Fig. 6 block diagram. INTERESTIM2 does not have any timer keeping track of stimulation pulse width. The duration of the stimulation pulses in this system are controlled externally by sending appropriate commands at suitable times. So the time resolution for stimulation pulses is a command frame period and depends on the maximum data transfer baud rate. INTERESTIM2 was laid out in a 3.6mm x 3.6mm area after a set of optimizations for the UofM 3μm BiCMOS process and sent for fabrication. The INTERESTIM2 layout is shown in Fig. 18.
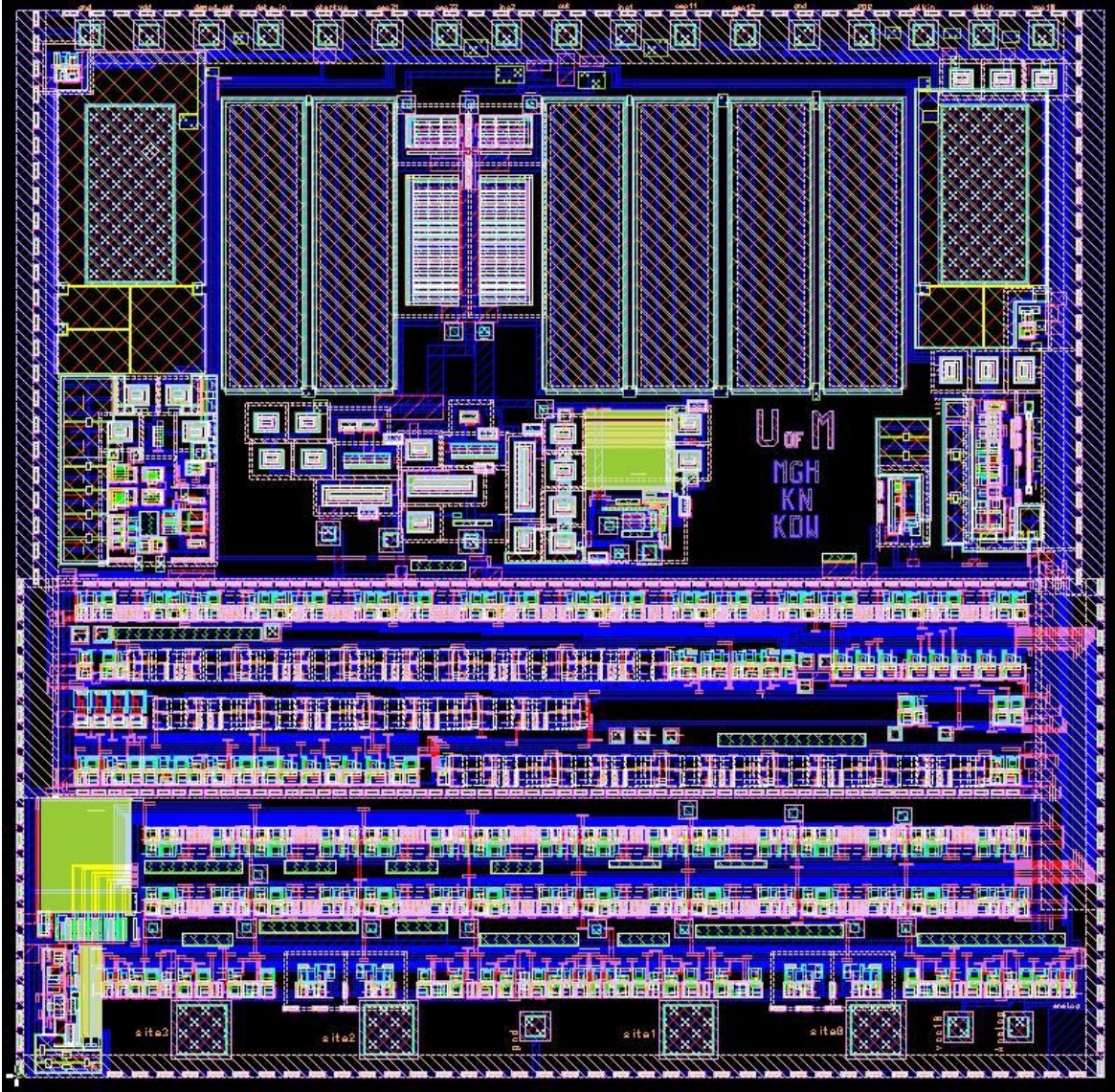
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Fig. 17: INTERESTI2 complete circuit schematic

Fig. 18: INTERESTIM2 layout

4. Conclusions

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